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EXAMINER	
MEW, KEVIN D	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,938	HERBST, JOSEPH	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 27* is/are rejected.

7)☒ Claim(s) *11-26, 28-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Action

Response to Amendment

1. Applicant's arguments/remarks filed on 4/8/2005 regarding claims 1-10, 27 have been fully considered and claims 1-33 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Headrick et al. (USP 5,724,358).

Regarding claims 1 and 27, Muller discloses a network switch to perform a method for storing data (ATM switch, see col. 3, lines 6-7 and element 82, Fig. 5) comprising:

at least one port data port interface (Buffering and Routing unit, see element 124, Fig. 5);

a first memory (a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178, see col. 7, lines 25-37 and Fig. 7 and Fig. 10);

a second memory (a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180, see col. 7, lines 25-37 and Fig. 7 and Fig. 10); and

a memory management unit (Buffer Manager unit and Routing and Buffering unit, see elements 128, 126, Figs. 5 and 7; note that the combination of Buffer Manager unit and Routing

and Buffering unit is interpreted as a memory management unit) in connection-with said at least one data port interface (Buffer Manager in connection with Routing and Buffering unit, see element 126, Fig. 5), said first memory (the Pointer Memory 178, see Fig. 7), and said second memory (Pointer Memory 180, see Fig. 7),

wherein the memory management unit (Buffering and Routing unit of the memory management unit, see element 126, Fig. 7) receives data from the at least one data port interface (Buffering and Routing receives data from the Input Translation, see Figs. 5 and 7), determines if the data is to be stored in one of the first memory or the second memory (a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7), stores the data in one of the first memory or the second memory as a linked list (pointer memories 178, 180, pointing to the Cell Buffer Memory, contain a plurality of linked list type data structures that are output queues for the plurality of output ports, see col. 8, lines 61-67), retrieves the data from one of the first memory or the second memory (data are retrieved from the corresponding cell buffers of the Cell Buffer Memory pointed to by pointer memories 178, 180 as output queues, see col. 8, lines 61-63), and forwards the data for egress (the Buffering and Routing unit 126 is forwarding the data for output to the Output Translation, see Fig. 5 and 7).

Regarding claim 2, Muller discloses a network switch as recited in claim 1, said network switch further comprising

a status location budget manager (Buffer Manager unit, see element 128, Figs. 7) in connection with the at least one data port interface (Buffering and Routing unit, see element 126, Fig. 7), the first memory (Pointer Memory 178, see Fig. 7), and the second memory (Pointer Memory 180, see Fig. 7), for determining if the data is to be stored in the first memory or the second memory (a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7).

Regarding claim 3, Muller discloses a network switch as recited in claim 1, said network switch further comprising

a first memory controller (Memory Manager 1, see element 170, Fig. 7) for storing data within said first memory (storing data pointed to by the Pointer Memory 178, see Fig. 7) and a second memory controller (Memory Manager 2, see element 172, Fig. 7) for storing data within said second memory (storing data pointed to by the Pointer Memory 180, see element 180, Fig. 7).

Regarding claim 4, Muller discloses a network switch as recited in claim 1, wherein said first memory further comprises on-chip memory (a memory buffer in the Cell Buffer Memory of

element 126 pointed to by Pointer Memory 178 is an on-chip memory with respect to the Cell Buffer Memory, see Fig. 7).

Regarding claim 5, Muller discloses a network switch as recited in claim 1, wherein said second memory further comprises off-chip memory (a memory buffer in the Cell Buffer Memory of element 126 pointed to by Pointer Memory 180 is off-chip memory with respect to the Buffer Manager 128, see Fig. 5).

Regarding claim 6, Muller discloses a network switch as recited in claim 1, wherein the memory management unit (Buffer Manager unit and Routing and Buffering unit, see elements 128, 126, Figs. 5 and 7; note that the combination of Buffer Manager unit and Routing and Buffering unit is interpreted as a memory management unit) further comprises

a communication channel (communication channel for data coming into data paths of the Buffering and Routing unit 126, see data arrow coming into element 126, Fig. 7);

a data input section (data path units of the Routing and Buffering unit receives data, see elements 182, 184, 186, 188, Fig. 7; note that data input section is interpreted to comprise Input Layer, Input Translation, Routing and Buffering, see Fig. 5) in connection with the communication channel (data paths in connection with the data arrow coming into element 126, Fig. 7);

a data output section (data path units of the Routing and Buffering unit outputs data, see elements 182, 184, 186, 188, Fig. 7; note that data output section is interpreted to comprise Output Layer, Output Translation, Routing and Buffering, see Fig. 5) in connection with the

communication channel (data paths in connection with the data arrow coming into element 126, Fig. 7);

a first memory controller (Memory Manager 1, see element 170, Fig. 7) in connection with the first memory (Memory Manager 1 in connection with a memory buffer in the Cell Buffer Memory of element 126 pointed to by Pointer Memory 178, see col. 7, lines 25-37 and Fig. 7 and Fig. 10, see Fig. 7), the data input section (Memory Manager 1 in connection with data paths receiving data via the Cell Buffer Memory, see elements 170, 182, 184, 186, 188, Fig. 7), and the data output section (Memory Manager 1 in connection with data paths outputting data via the Cell Buffer Memory, see elements 170, 182, 184, 186, 188, Fig. 7);

a second memory controller (Memory Manager 2, see element 172, Fig. 7) in connection with the seond memory (Memory Manager 2 in connection with a memory buffer in the Cell Buffer Memory of element 126 pointed to by Pointer Memory 178, see col. 7, lines 25-37 and Fig. 7 and Fig. 10), the data input section (Memory Manager 2 in connection with data paths receiving data via the Cell Buffer Memory, see elements 172, 182, 184, 186, 188, Fig. 7), and the data output section (Memory Manager 2 in connection with data paths outputting data via the Cell Buffer Memory, see elements 172, 182, 184, 186, 188, Fig. 7);

at least one address pool (Free List Memory, see col. 7, lines 14-17 and element 176, Fig. 7; Free List Memory stores a plurality of pointers linking all free locations in cell buffer memory together so that a list of every free memory location is available) in connection with the first memory controller (Memory Manager 1, Fig. 7) and the second memory controller (Memory Manager 2, see Fig. 7); and

a scheduler (Memory Manager 1 schedules output queues for ports 0 through 7 to be stored in pointer memory 178, see col. 7, lines 1-3 and col. 8, lines 66-67) in connection with the data input section (data path units receiving data, see elements 182, 184, 186, 188, Fig. 7) and the data output section (data path units outputting data, see elements 182, 184, 186, 188, Fig. 7).

Regarding claim 7, Muller discloses a network switch as recited in claim 6, wherein the data input section further comprises:

a cell assembly unit (Output Translation System for assembling ATM cells, see col. 6, lines 9-27 and element 130, Fig. 5) in connection with the communication channel (communication channel for data coming into data paths of the Buffering and Routing unit 126, see data arrow coming into element 126, Fig. 7);

a status location budget manager (Buffer Manager, see element 128, Fig. 7) in connection with the cell assembly unit (Buffer Manager is in connection with the Output Translation via the CPU, see element 130, Fig. 5) ;

at least one cell accumulation buffer (Routing and Buffering unit) in connection with the status location budget manager (Buffer Manager, see elements 128, 126, Figs. 5 and 7);

a slot assembly unit (Output Layer 132 to convert ATM cells into serial format, see col. 6, lines 9-27 and Fig. 5) in connection with the at least one cell accumulation buffer (Output Layer is in connection with the Routing and Buffering unit via the Output Translation, see Fig. 5) and said second memory controller (Output Layer is in connection with the Memory Manager 2 via the Routing and Buffering unit, see Figs. 5 and 7); and

at least one address pool (Free List Memory, see element 176, Fig. 7) in connection with the status location budget manager (Buffer Manager, see Fig. 7), the slot assembly unit (Free List Memory in connection with Output Layer 132 via the Routing and Buffering unit, see Figs. 5 and 7) and the data output section (Free List Memory in connection with the data output section comprising Output Translation 130, Output Layer 132 via the Routing and Buffering unit, see Figs. 5 and 7).

Regarding claim 8, Muller discloses a network switch as recited in claim 7, wherein the cell assembly unit converts data received from the communication channel into a cell header format (ATM cell has header field HEC, see col. 6, lines 15-17 and Fig. 4), a cell data format (information field, see Fig. 4), and a sideband information format (PT field distinguishes between cells containing user data and network information, see col. 5, lines 1-38 and Fig. 4).

Regarding claim 9, Muller discloses a network switch as recited in claim 7, wherein the status location budget manager (Buffer Manager, see element 128, Fig. 7) determines whether data received by the cell accumulation buffer is to be stored in the first memory or the second memory (a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 7-15, see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7).

Regarding claim 10, Muller discloses a network switch as recited in claim 7, wherein the at least one cell accumulation buffer collects data (Routing and Buffering unit collects data, see Fig. 7) to be stored in the second memory (stores data in buffer pointed to by Pointer Memory 180 in the Cell Buffer Memory, see Fig. 7) prior to sending the data to be stored in the second memory to the slot assembly unit (data are stored in buffer pointed to by Pointer Memory 180 in the Cell Buffer Memory prior to sending the data to the Output Layer 132, see Fig. 7).

Response to Arguments

3. Applicant's arguments filed on 4/8/2005 have been fully considered but they are not persuasive.

With respect to applicant's argument that Headrick fails to discloses or suggest that the memory management unit determines if the data is to be stored in the first memory or the second memory, the Examiner respectfully disagrees. As cited on page 3 in the previous Office Action, Headrick discloses a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 178 is determined to be used by the Buffer Manager to store data cells for ports 0-7, and a memory buffer in the cell buffer memory of element 126 pointed to by Pointer Memory 180 is determined to be used by the Buffer Manager to store data cells for ports 8-15 (see col. 7, lines 1-3, 25-37, col. 8, lines 61-67, col. 9, line 1, and Fig. 7). In other words, each port (ports 0-7, 8-15) is associated with a respective pointer memory that is controlled by the memory managers to determine a memory location in the cell memory buffer 174 pointed to by the respective pointer memory. Therefore, ATM/data cells that are destined to one of ports 0-7, or ports 8-15 will be stored in the cell buffer memory pointed to by the respective pointer

memory, which is either pointer memory 178 or pointer memory 180. This means that the buffer memory managers will determine data cells that are destined to ports 0-7 will be stored in a first memory location in the cell buffer memory 174 pointed to by memory pointer 178, and data cells that are destined to ports 8-15 will be stored in a second memory location in the cell buffer memory 174 pointed to by memory pointer 180. This reads on the limitation that "the memory management unit determines if the data is to be stored in one of the first memory or the second memory" of claim 1.

Applicant further argued that Headrick fails to discloses or suggest that the memory management unit stores data in the first memory or the second memory as a linked list, the Examiner again respectfully disagrees. As cited on page 3 of the previous Office Action, Headrick discloses pointer memories 178, 180, which are interpreted as being first memory and second memory, contain a plurality of linked list type data structures (see col. 8, lines 61-67).

In light of the reasoning above, claims 1-10, 27 stand rejected under 35 U.S.C. 102(e) as being anticipated by Headrick et al.

Allowable Subject Matter

4. Claims 11-26, 28-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In claim 11, a network switch as recited in claim 7, wherein the slot assembly unit receives cells from the cell accumulation buffer and packages the received cells into cell slots to be stored in the second memory.

In claim 12, a network switch as recited in claim 6, wherein the data output section further comprises:

a cell disassembly unit in communication with the communication channel;

a cell retrieval and reclaim unit in communication with the cell disassembly unit; and

a read buffer and slot disassembly unit in communication with the cell retrieval and reclaim unit and the second memory controller.

In claim 17, a network switch as recited in claim 7, wherein said at least one address pool further comprises

a cell free address pool connected to the first memory controller; and

a slot free address pool connected to the second memory controller.

In claim 18, a network switch as recited in claim 6, said network switch further comprising:

a cell free address pool unit connected to the first memory controller;

a slot free address pool unit connected to the second memory controller; and

a scheduler connected to the first memory controller and the second memory controller.

In claim 28, a method for storing data in a network switch as recited in claim 27, wherein the determining step further comprises the steps of:

determining if a cell count is less than a first predetermined threshold for the egress;

determining if a number of cells in the second memory is zero; and

determining if a number of cells in the first memory added to a number of cells remaining in an assembly is less than the first predetermined threshold.

In claim 31, a method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the second memory further comprises the steps of initializing global storage of data and continuing global storage of data until a last slot is stored.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WELLINGTON CHIN
RVISORY PATENT EXAMIN

KDM
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